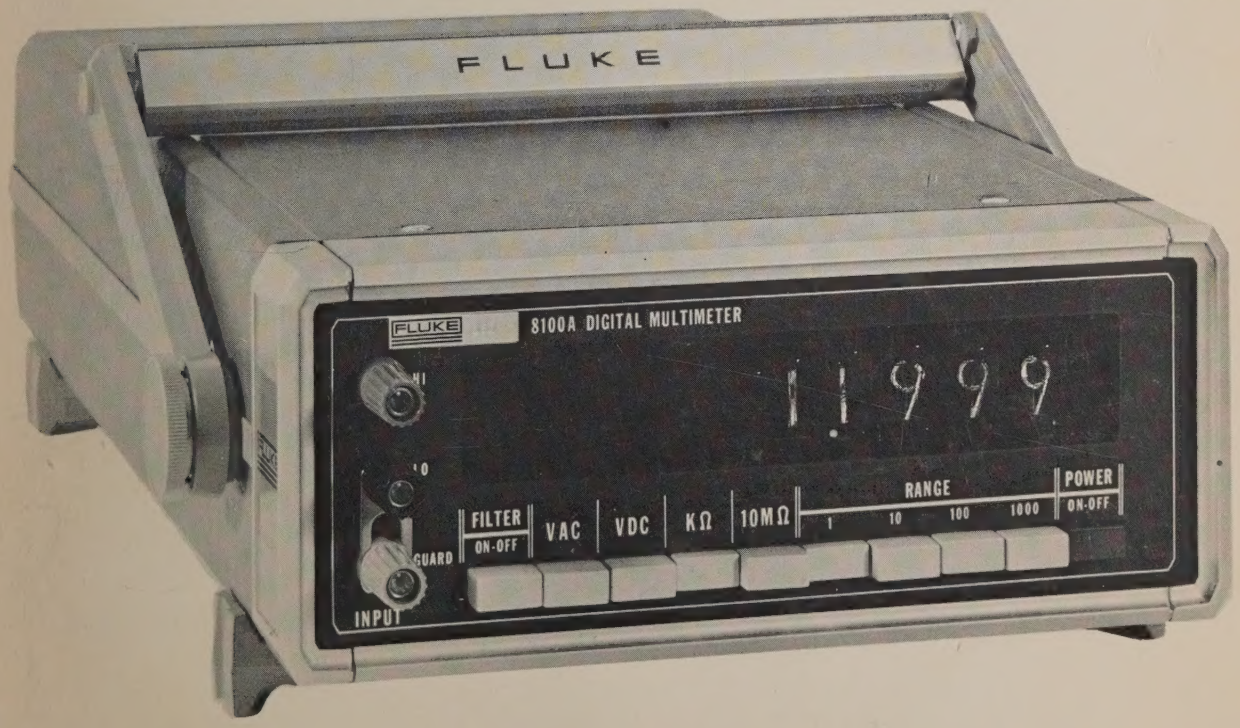
Electronic Services - Los Angeles
M17557X

model 8100

DIGITAL MULTIMETER



FLUKE®

STUDENT HANDOUT

Introduction

This training course has been prepared by the Customer Service Department of the John Fluke Mfg. Co., Inc. to assist the experienced technician to understand how the instrument works, how to calibrate it and how to maintain it. This manual is intended as a supplement to the Audio/Visual training package of the same title. It is suggested that prior to attending this course of instruction, the course titled "Recirculating Remainder" should have been completed. Should you have any questions, comments or suggestions about this course of instruction please feel free to communicate them to the Training Department by letter or telephone.

Customer Service Training Dept.

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8100A DIGITAL MULTIMETER OPERATIONAL THEORY

The 8100A consists of three main sections, referring to Figure 1 and the Schematic Drawings.

1. The Buffer section acts as a signal conditioner, capable of dividing voltage inputs, filtering and impedance conversion. The input divider also functions as a portion of the current source in the resistance ranges. (See Figure 2)

2. The Analog/Digital Conversion system, accepts the output from the Buffer and digitizes it using FLUKE'S Recirculating Remainder system of conversion. The unit samples three times a minute and recycles every 20 milliseconds.

3. The display section accepts the BCD output of the Analog to Digital Converter and puts it into ten line decimal output and displays the result on NIXIE tubes on a timed pulse basis.

In addition to the three main sections described above, the Power Supply serves dual functions. (See Figure 3 and Schematic No. 4). In addition to supplying the voltages required by the instrument it also contains an inverter that is used to both produce operating voltages for the instrument and supply the clock or synchronization for timing the instrument.

Power for the 8100A is supplied by either the AC power line or via the internal battery pack, as furnished with the −01 option. When operated from line voltage transformer, T101 provides two outputs. One output is rectified and filtered and used for the −18 volt supply in the instrument. The other winding provides a higher voltage which is rectified and used to charge the battery option, through DS11 which acts as a series limiting element.

The voltage supplied by the line voltage conversion is always greater than the voltage from the batteries, back biasing CR34 which prevents draining the batteries. The negative voltage, from either the batteries or the rectifiers CR1 and CR2, is regulated and filtered after passing through the protective fuse, F2, and then on to supply the instrument all of it's negative voltage needs.

The −18 volts operates a 250 Hz inverter consisting of Q4, Q5 and a driver transformer T102. The output voltages from T102 are then conditioned to supply the remaining potential needs of the 8100A.

A high voltage winding (100V) operates a doubler rectifier circuit which provides 200V dc. This +200V dc is used to pulse the readout tubes.

T102 also provides one output which is rectified and filtered to +5 volts which is used to supply all of the integrated circuit logic. Another winding of T102 provides a voltage which is rectified and regulated to provide the +15 volts needed as a positive supply in the instrument. This +15 volts is further dropped by a zener regulated circuit to provide the +7.0 volt reference needed in the 8100A. This +7.0 volt reference supply has a fixed load of 2 ma in R181 and is protected from current reversals when an overload occurs in the ohms configuration by CR10.

INPUT RANGE DIVIDER (Figure 2 and Schematic No. 1)

The function switching on the front panel will provide one of the four basic configurations shown in Figure 2. When the instrument is operated in the DC volts position the divider will provide divisions of 1, 10, 100 and 1000 in order to maintain a 1 volt input into the Buffer. The input divider consists of R156, R158, R159, R160 and R157 is provided for calibration.

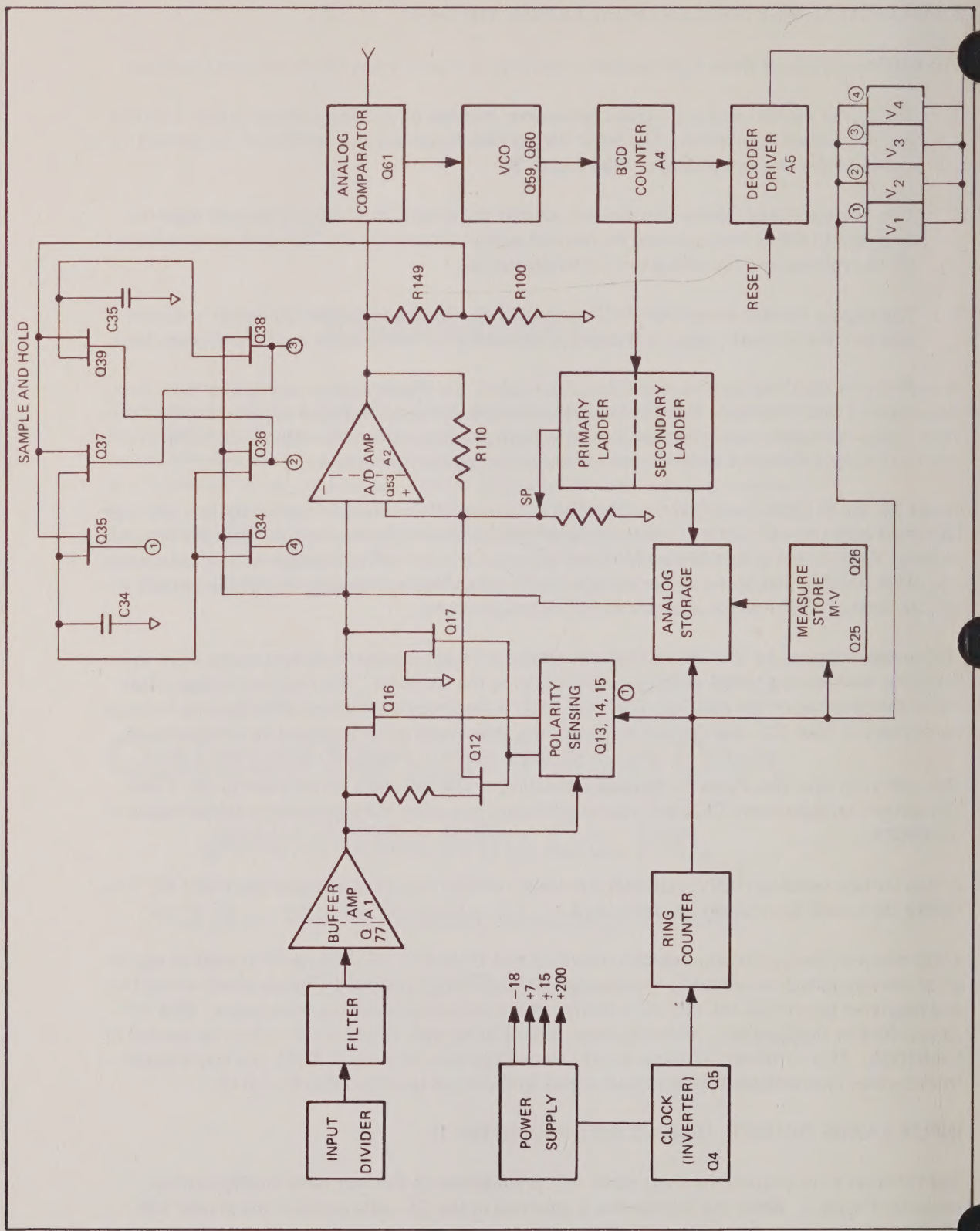


Figure 1. 8100 BLOCK DIAGRAM

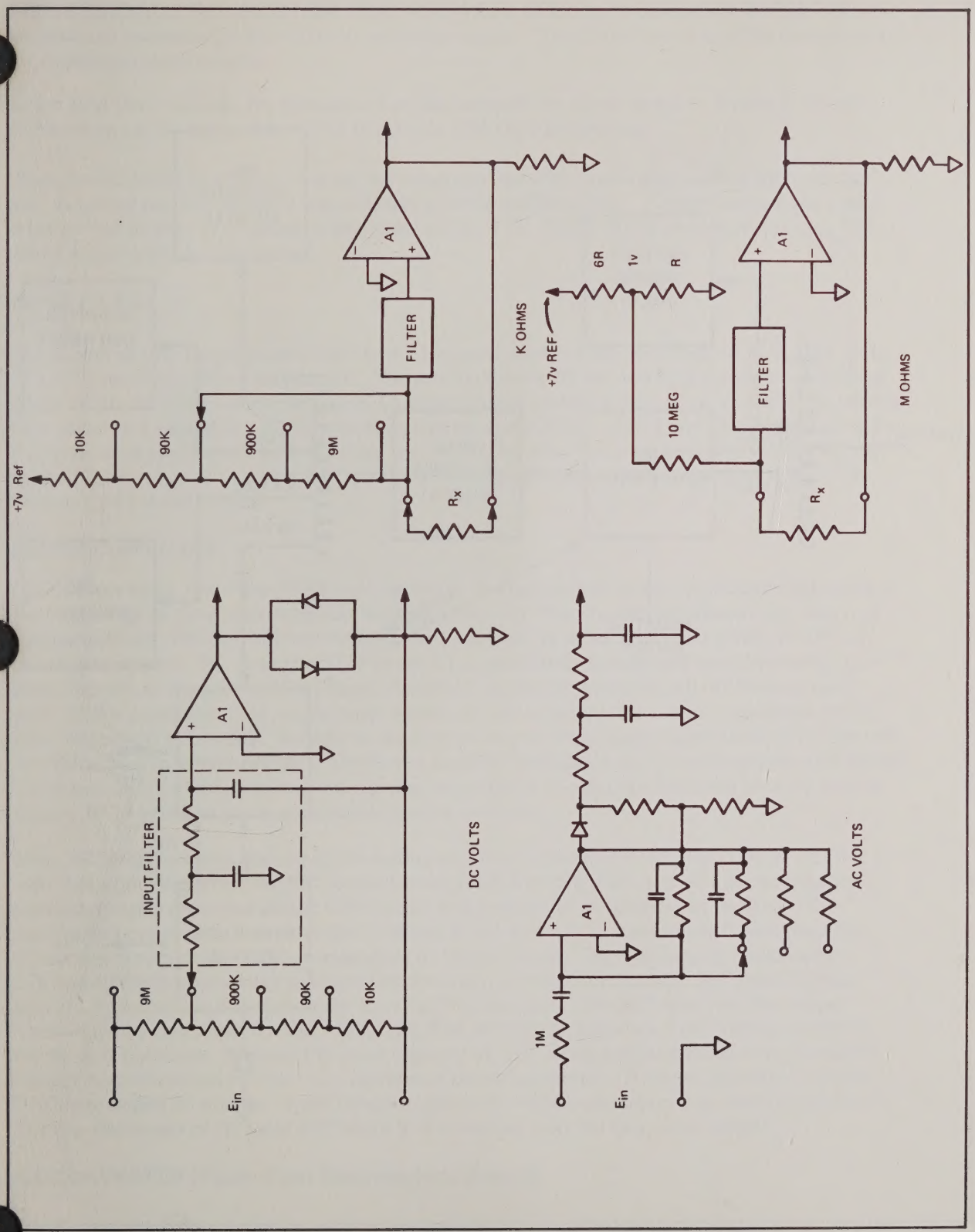

+7v Ref
10K
90K
900K
9M
A1
FILTER
R_x
K OHMS
+7v REF
6R
1v
R
10 MEG
M OHMS
INPUT FILTER
DC VOLTS
AC VOLTS
1M
E_{in}

Figure 2.

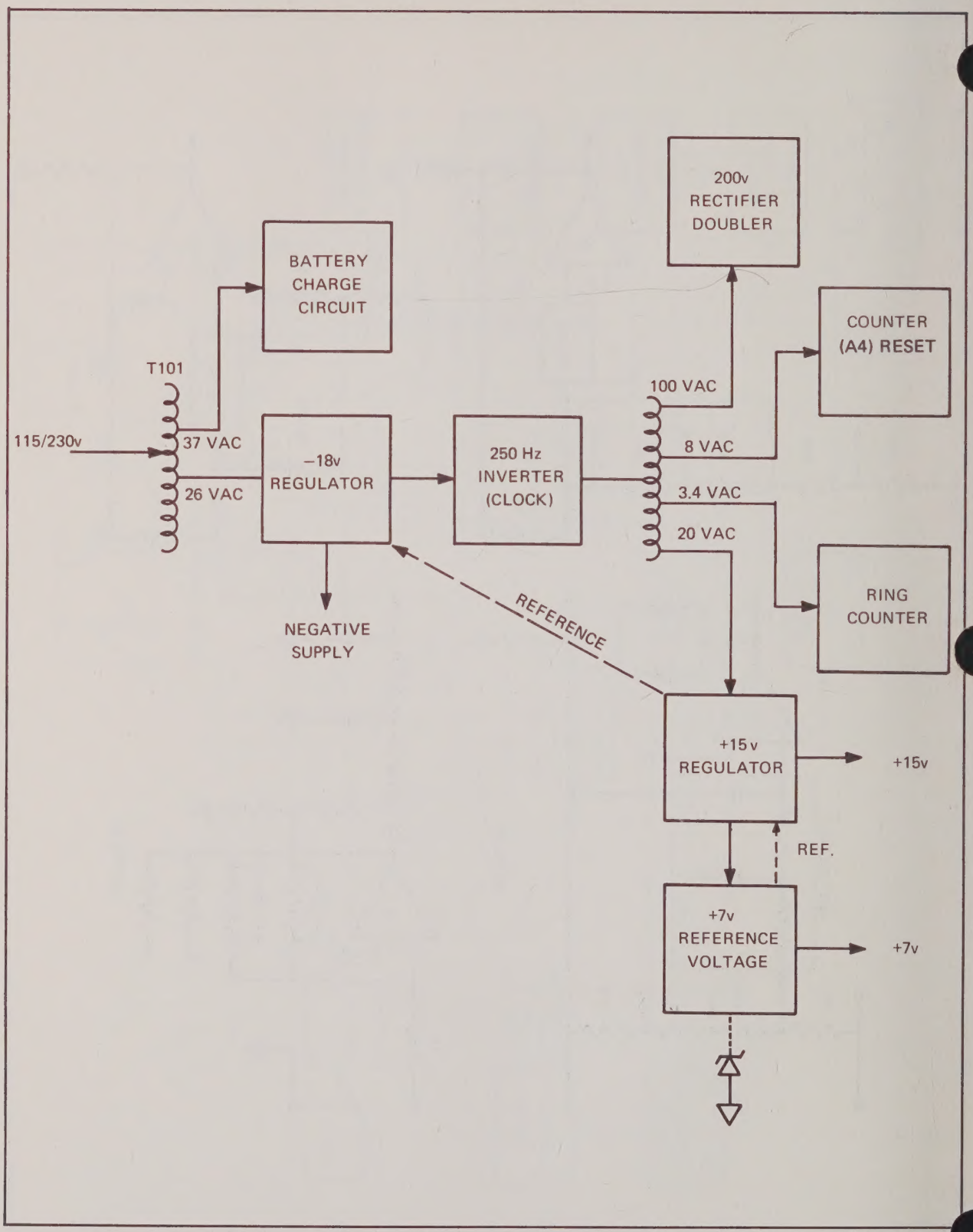


Figure 3. 8100 POWER SUPPLY

In the K Ohms function, the bottom of the input divider (R160) is removed from the common binding post and connected to the +7.0 volt reference supply. The divider now acts as the current supply for resistance measurements.

In the 10M Ohm function the bottom end of the range divider is connected to divider R152 and R154 which can be adjusted by R153 to provide 10M Ohm calibration.

When the AC Volts function is selected the input configuration is changed to an operational rectifier. A pair of rectifier diodes is placed inside a strong feedback loop. A negative feedback signal proportional to the input voltage is developed across R161, R162, R174 and calibration pot R34, which is fed to the A-D Amplifier.

INPUT FILTER

The output of the Range Divider is fed into a two pole, passive filter consisting of R27, R28, C10, C11, C12 and C13. (Filter switch out). The settling time is .25 sec and 60 Hz is attenuated about 20 db. With the Filter switch depressed, C10 and C13 are removed from the circuit and the settling time becomes 1 second and 60 Hz is now attenuated about 60 db. CR11 and CR12, together with R27 provide protection for both the filter and the Buffer amplifier from excessive voltage inputs. In the 10 volt range, R27 is switched out since the output impedance of the range divider is 1M Ohm and R27 is not needed.

BUFFER AMPLIFIER

Q77 is a low noise, low drive J-FET pair, operating in a common source configuration and serves as the input stage to the Buffer Amplifier configuration. R175 is the zero adjustment pot, which in conjunction with R176, R177 and R188 forms a network by which the initial offset of Q77 can be reduced to zero. The output of Q77 drives A1, a monolithic operational amplifier, which provides the bulk of the gain. C51 is placed around A1 to provide a smooth roll off through unity gain. Q79 is a common base output stage whose purpose is to raise the output impedance of the amplifier as high as possible. In order to avoid degrading the high output impedance, Q79 operates into a constant load current, Q80. The Buffer amplifier feedback loop is completed through diodes CR14 and CR15, which provide a voltage step around zero to drive the following polarity sensing circuit. R174 provides the load resistance for the amplifier.

When AC Volts function is selected, the buffer amplifier is connected as an operational rectifier with R24 as the input resistor, AC coupled through C9 and R29, R30, and R32 as the negative feedback ranging resistors. Diodes CR14 and CR15 now act as an operational rectifier. The positive half cycles only flow through CR15 and R162 where they develop a half wave rectified DC voltage proportional to the average value of the AC input. The high output impedance of Q79 and Q80 aids appreciably in improving the linearity at low levels where the threshold voltages of CR14 and CR15 tend to lower the amplifier loop gain. The half wave rectifier output is smoothed by two stage RC filter R35, C19, R36 and C20 to provide a 1 volt full-scale output for the A-D Converter. Because the input capacity of Q77, along with additional stray capacities, causes an additional pole in the loop response of the AC converter. Trimmer capacitors C14 and C15 are provided on the two lowest ranges to adjust the frequency response up through 20 kHz. The low resistances of R31 and R32 make this unnecessary on the two upper ranges.

A-D CONVERTER (Figure 1 and Schematic No's. 2 and 3)

The Recirculating Remainder conversion process is synchronously operated. That is to say; it progresses through it's steps in time with an internal clock, which is the Power Supply Inverter (250 Hz).

A Ring Counter fed by one of the outputs of T102, divides each cycle into five time periods of 4 milliseconds each as shown in Figure 4. The first time period is the ZERO time, this is the time period when the offset is removed from the A-D Converter amplifier. During the remaining four time periods each of the four digits is digitized and then displayed. At the end of the last period, the Ring Counter supplies a synchronizing pulse through R68 and C27 to the Measure Store Multivibrator Q25. It is the job of the Measure Store circuit to determine whether the A-D Converter will sample (Measurement Mode) the input voltage or continue to display the information held in storage (Storage Mode). See Figure 5 for sequence of operation.

POLARITY SENSING

Q13 turns on only when a 1 period time pulse appears at its gate and in Measurement Mode. This activates the Polarity Sensing Circuit. If the voltage at R40 is positive (Negative instrument input) Q15 will conduct and the signal from the Measure Store Multivibrator (Q25) will cause FET switch Q16 to conduct placing input on the A-D Amplifier.

If the voltage sensed by R40 is negative (Positive input to the 8100) Q14 will conduct and the signal at the collector of Q14 and the pulse from the Measure Store Multivibrator Q25 will turn FET switches Q12 and Q17 on. The negative output of the Buffer will be applied through the scaling resistors R50 and R51 and switch Q12 to the positive input of the A-D Amplifier. The Polarity Detector operates only while the instrument is in the Measurement Mode of operation and serves no function in the Storage Mode.

During time period 1, the amplified remainder is applied to C34. Q35 is prevented from conducting during the first half of the time period by the clock signal which is coupled through CR36 to its gate. During the second half of the period Q35 is ON and the amplified remainder is applied to C34.

During the second time period, Q35 is OFF and Q36 is ON which applies the remainder stored in C34 to be applied to the input of the Amplifier. Q39 is switched ON and the remainder is now applied to C35. Q39 is switched OFF during the third time period and Q37 and Q38 are switched ON which allows the remainder stored in C35 to be applied to the amplifier input.

During the third time period the remainder is stored in C34.

During the fourth and last time period Q34 is switched ON and the final remainder stored in C34 is applied to the input of the Amplifier.

ANALOG STORAGE

Clock pulses being applied through CR19 and Q28 allow conduction only during the second half of each time period. Q30 through Q33 are enabled only during the time period pulse corresponding to its gate connection.

During the last half of the 1 period the output of the Secondary Ladder is stored in capacitor C30. During the last half of the second period, the output of the Secondary Ladder is stored in C31. Etc.....

Q29 is enabled only when the instrument is in the Storage Mode and allows the output of each of the storage capacitors to appear at the input to the amplifier.

Analog storage is used only when the instrument is in the Storage Mode of operation as determined by the Measure Store Multivibrator.

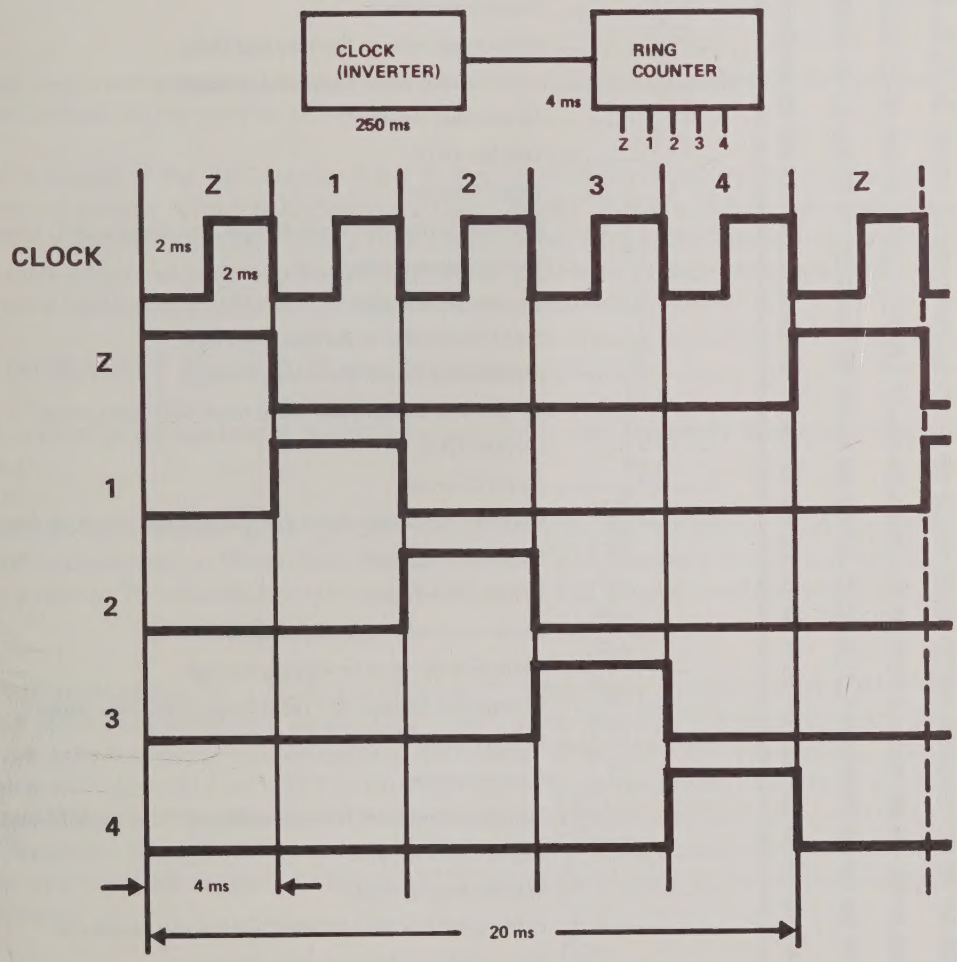


Figure 4. 8100 TIMING DIAGRAM

MEASURE MODE

Z — Internal error correction. (Offset removal)
1 — Sample input
1 — Sense and switch polarity
1 — Digitize first digit
1 — Display first digit
1 — Store remainder in Sample and Hold
1 — Store analog value in Analog Storage
1 — Disconnect input
1 — Display OUT
1 — Reset Counter
2 — Connect remainder from Sample and Hold to A/D Amplifier
2 — Digitize second digit
2 — Display second digit
2 — Store remainder in Sample and Hold
2 — Store analog value in Analog Storage
2 — Disconnect Sample and Hold from A/D Amp. input
2 — Display OUT
2 — Reset Counter
3 — Connect remainder from Sample and Hold to A/D Amp.
3 — Digitize third digit
3 — Display third digit
3 — Store remainder in Sample and Hold
3 — Store analog value in Analog Storage
3 — Disconnect Sample and Hold from A/D Amp. input
3 — Display OUT
3 — Reset Counter
4 — Connect remainder from Sample and Hold to A/D Amp
4 — Digitize fourth digit
4 — Display fourth digit
4 — If the fourth is the last digit, ignore any remainder
4 — Store analog value in Analog Storage
4 — Disconnect Sample and Hold from A/D Amp. input
4 — Display OUT
4 — Reset Counter

NOTE: Depending on the state of the Measure Store Multivibrator the instrument will return to "Z" time in either Measure Mode (unusual case) or enter Storage Mode.

Figure 5. 8100 DISPLAY SEQUENCE, MEASURE MODE

MEASURE STORE MULTIVIBRATOR

The one shot multivibrator formed by Q25 and Q26 has dual synchronizing inputs. The Measurement Cycle (approx. 20 ms) is coincident with the conduction of Q25. The Storage Cycle (approx. 330 ms) is coincident with the conduction of Q26. The multivibrator is triggered at the end of each complete cycle by the negative edge of the 4th time period pulse. If C29 is sufficiently discharged, this negative pulse will cause the multivibrator to pulse, sending a 20 ms measure pulse to the Polarity Sensing circuit which starts a measurement cycle. If the multivibrator does not pulse the 8100 remains in Storage Mode.

DISPLAY

It should be noted that each readout tube is on only during the last half of its corresponding time period. (2 ms on and 18 ms off).

The BCD output of the A4 Counter is fed to the Decoder Driver where it is translated into decimal output. If the BCD code was 3 the Decoder Driver will apply ground to the three line to all readout tubes. The 1 time period pulse, in conjunction with the clock pulse,which occurs only during the second half of each time period, will enable Q67 and Q71 thus allowing the +200 volts to light the three digit in V1.

EXAMPLE OPERATION (Figure 6) (Example voltage is .6532V)

Counter A4 is reset to zero as it is at the beginning of every time period by the pulse from A3A NAND gate.

The Ring Counter produces the ZERO pulse and Q18 and Q58 are turned on. Q58 connects C37, the zero holding capacitor, to the output of amplifier A2. Q18 connects the positive input of the amplifier to ground. This operation removes the offset for the remainder of the measurement cycle.

The Ring Counter produces the 1 time period pulse. It is necessary to assume that Q25 in the Measurement Store Multivibrator is conducting. The 1 pulse will turn transistor Q13 on. Since the .6532 volts into the instrument is positive, the voltage across R40 will be negative. Q14 will conduct which will cause Q12 and Q17 to turn on. These transistors were enabled by the Measure pulse from the Measure Store Multivibrator. The negative voltage from the Buffer will be applied to the A-D Amplifier through scaling resistors R50 and R51. Q17 connects the positive input to the amplifier to ground via resistors R186 and R187 which provide offset correction voltage to the positive input.

With R98, 200 kΩ, in the feedback loop and R51 and R50 as the input resistance the gain of the amplifier is 70. Q52 is used as temperature compensation only.

With .6532 volts at the input terminal of the amplifier, the output will attempt to go to 40 volts to satisfy the loop gain, but will be prevented from going so high by the limiting action of Q76 and R110. The output will exceed 7.0 volts and cause the Analog Comparator to conduct.

The Analog Comparator, Q89, will generate current at any time the voltage output of the Amplifier is seven or more volts. The current that it supplies is fed to the Voltage Controlled Oscillator.

MEASURE MODE	ZERO	1	2	3	4
Q18 & Q58 conduct and remove offset from A-D amp.	▬				
1 from Ring Counter enables Q13, polarity is determined and input FETs apply .6532 to A-D. 6 is digitized, remainder is stored in S & H C34. 6 is displayed and .6v stored in C30.		▬ ▬			
Input is disconnected from A-D amplifier.					
.532v from C34 is applied to A-D input. 5 is digitized and remainder .32 is stored in S & H C35. 5 is displayed and .5v is stored in C31.			▬ ▬		
.32 from C35 is applied to A-D amplifier. 3 is digitized and remainder .2 is stored in C34. 3 is displayed and .3v is stored in C32.				▬ ▬	
.2v from C34 is applied to A-D input and digitized. 2 is displayed and .2v is stored in C33.					▬ ▬
STORAGE MODE	**ZERO**	**1**	**2**	**3**	**4**
Q18 & Q58 conduct and remove offset from A-D amp.	▬				
Q30 conducts and applies .6v from C30 to A-D amp. 6 is digitized 6 is displayed and .6v is restored to C30.		▬ ▬			
Q31 conducts and applies .5v from C31 to A-D amp. 5 is digitized 5 is displayed and .5v is restored to C31.			▬ ▬		
Q32 conducts and applies .3v from C32 to A-D amp. 3 is digitized. 3 is displayed and .3v is restored to C32.				▬ ▬	
Q33 conducts and applies .2v from C33 to A-D amp. 2 is digitized. 2 is displayed and .2v is restored to C33.					▬ ▬
NOTE: If C29 is sufficiently discharged, the negative going portion of the 4 pulse will trigger the Measure Store Multivibrator and a measure pulse will be generated and a measure cycle will be started. If not another storage cycle will start.					

Figure 6.

The Voltage Controlled Oscillator, Q59 and Q60, will supply a series of pulses when supplied current. The repetition rate will be proportional to the current being supplied.

The pulses from the VCO are applied to the Counter A4, which is reset at the start of each time period. This counter translates the pulses into Binary Coded Decimal output. This BCD output is applied to the Ladder Switches and Drivers. As the BCD numerical value increases, the ladders produce 0.1 volt steps in their output. Thus in this case when the Primary Ladder output reaches .6 volts and is fed back to the input of the A-D Amplifier, the input difference to the amplifier becomes .0532 volts and the output of the amplifier will be less than 7 volts. When this occurs the Analog Comparitor Q89 does not furnish current to the VCO which causes it to stop pulsing.

The Decoder Driver translates this BCD output to decimal and produces a ground potential that is fed to all of the readout tubes 6 line. Only the 1 tube will light since it is the only one enabled by both clock and the 1 pulse via Q67 and Q71.

The Secondary Ladder feeds the Analog Storage circuit. Q28 is enabled only during the second half of each time period and Q30 is enabled by the 1 time period pulse. This causes C30 to be charged to .6 volts being furnished by the Secondary Ladder.

The remainder voltage during time period 1 was 0.532 volts at the input to the A-D Amplifier. This remainder is multiplied by the amplifier to 3.724 volts and appears across remainder resistors R99, R100 and R149. It is apparent that the total resistance is 14 Ω and that 2 kΩ represents 1/7 of the total resistance. This means that one seventh of the voltage appearing across the total remainder resistance appears across R100. This means, in the example case, .532 volts. This voltage will be applied across C34 in the Sample and Hold Circuit by the 1 time period pulse enabling transistor Q35. CR36 allows Q35 to be enabled only during the second half of the time period.

SUMMARY:

The highlights of the action that has taken place during the first time period are as follows:

1. The .6 volt was digitized.
2. .6 volt was placed in Analog Storage.
3. The remainder voltage .532 was placed in Sample and Hold.
4. The 6 was displayed during the last half of the time period by V1.

Time period 1 ends and transistor Q13 is no longer enabled as the 1 pulse is no longer furnished to it.

At the start of time period pulse 2 enables Q36 which applied the .532 volt remainder stored in C34 to appear at the input to the A-D Amplifier via Q18 which is enabled for the entire duration of The Measure Cycle. The .532 volts are amplified by 70 and once again the output of the amplifier exceeds the 7 volt reference causing Q89 to furnish current to the Voltage Controlled Oscillator. The pulse train produced is translated to BCD output and the Ladders are switched up in 0.1 volt increments until .5 volts is fed from the Primary Ladder to the summing junction of the A-D Amplifier. The input to the amplifier at this time is 0.32 volts which results in an output from the amplifier that is less than 7 volts and Q89 cuts off. The

BDC output from the A4 Counter is applied to the Decoder Driver and translated to decimal output, placing ground potential on all of the "5" lines to the readout tubes. The clock and 2 pulses enable Q68 and Q72 during the last half of the time period. Thus the readout tube V2 will display the "5" only during that last half of the time period.

The Secondary ladder will have an output of .5 volts at this time and it will be stored on capacitor C31 during the last half of the time period when Q28 conducts and Q31 is enabled by the 2 pulse.

The remainder, .032 volts will be amplified and divided by the remainder resistors and will be stored in the Sample and Hold circuit capacitor C35 via the enabled Q39 as .32 volts.

During period "3" Q38 will be enabled and apply the .32 volts, stored there, across the input to the A-D Amplifier through Q27.

The amplified voltage from the output of the amplifier will exceed the 7 volts of reference and Q89 will supply current to the Voltage Controlled Oscillator which will start a pulse chain. The pulses will be translated into BCD output. The BCD output will switch both Ladders and be decimalized by the Decoder Driver. When the output of the Primary Ladder reaches .3 volts the output of the amplifier will be less than 7 volts and Q89 will stop supplying current to the VCO. The decimalized "3" will appear as a ground potential on all of the 3 lines to the readout tubes. During the last half of the time period the +200 volts will be applied to V3 via Q69 and Q73 being enabled by the clock pulse and the 3 pulse thus allowing V3 to display the digit 3.

The .3 volts from the Secondary Ladder will be stored in Analog Storage capacitor C32 during the last half of the time period when Q28 is enabled and the 3 pulse has enabled Q32.

The remainder .02 at the input of the amplifier is amplified and appears across the remainder resistors and will be divided down to .2 volts and Q37 will be enabled causing this remainder to be stored in C34.

During time period 4 Q34 conducts applying the .2 volts stored in C34 to appear on the input to the A-D Amplifier. The output will exceed the reference voltage causing Q89 to supply current to the VCO which will start a pulse train. Counter A4 will count the pulses and translate them to BCD output. This BCD output causes the Ladder switches to operate and the output from the Primary Ladder is fed back to the summing point of the A-D Amplifier. When the output reaches .2 volts, the output of the amplifier is no longer higher than 7 volts and Q89 will stop conducting. The VCO stops pulsing and the Decoder Driver will translate the BCD output to decimal and apply ground potential to the 2 lines of all of the readout tubes. The clock and 4 pulses will enable Q70 and Q74, which will allow the +200 volts to light the tube V4 during the second half of the time period. The Secondary Ladder will have an output of .2 volts which will be stored in Analog Storage capacitor C33, the 4 pulse having enabled Q33 and the second half time period pulse having enabled Q28.

This completes a Measurement Cycle. As the 4 time pulse goes negative returning to zero potential it will cause Q25 (Measure Pulse) to conduct, only if capacitor C29 is sufficiently discharged. In this case it would not be possible for the instrument to start another Measurement Cycle as C29 would be fully charged.

SUMMARY:

It will be noted that each increment of voltage has been stored in the Analog Storage capacitor as follows:

C30 .6 volts
C31 .5 volts
C33 .2 volts

None of these stored voltages were used in the Measurement Cycle. C29 was fully charged and Q26 is conducting, which occurs during the Storage Cycles of the instrument. Q27 will be off and Q29 will be enabled until the Measure Store Multivibrator is operated again. Q26 will conduct for approximately 330 ms or about 16 cycles of the instrument. At that time C29 will be sufficiently discharged to allow Q25 to conduct when it receives a negative going pulse from the 4th time period pulse. Q25 will then conduct for approximately 20 ms or one Measurement cycle.

STORAGE CYCLE (Figure 7)

The ZERO pulse will again cause the offset to be removed from the A-D Amplifier by placing C37 across the output of the amplifier and grounding the input, as the result of Q18 and Q58 conducting.

The 1 pulse will cause Q30 to enable and the voltage stored on C30 (0.6 volts) to be applied to the input of the A-D Amplifier through Q29, which has been enabled by the Measure Store Multivibrator.

The A-D Amplifier amplifies the .6 volts by 70 and the output of the A-D Amplifier exceeds the 7 volt reference causing Q89 to conduct and supply current to the VCO. The VCO will start producing a pulse train. These pulses are counted and translated into BCD output by the action of Counter A4. The BCD output causes the Ladders to switch and increase their output by .1 volt per pulse. When the output of the Primary Ladder reaches .6 volts it will cause the A-D Amplifier to be satisfied and it will no longer have an output that is above the 7 volt reference of the instrument. The Secondary Ladder will have produced a .6 volt output which will be stored in C30 during the second half of the time period via Q28.

The Decoder Driver will have translated the BCD output to decimal and applied ground to all of the readout lamps on the 6 line. Q67 and Q71 are enabled, during the second half of the time period, by the clock and 1 pulses thus applying the +200 volts to V1 enabling it to display the 6.

During time period 2, Q31 and Q29 will conduct causing the .5 volts stored in C31 to appear across the input to the A-D Amplifier. The amplifier will have an output of more than 7 volts, which will cause Q89 to conduct and supply current to the VCO, which will produce a pulse train. The Counter A4 will count and translate the output to BCD. The Ladders will produce .1 volt of output for every pulse. The Primary Ladder being fed back to the input of the A-D Amplifier will cause the output of that amplifier to drop below 7 volts when .5 volts level is reached, which will cause Q89 to cut off and the VCO to stop producing pulses.

The Secondary Ladder will have produced .5 volts which will be stored on C31 during the second half of the time period by the conduction of Q28. The Decoder Driver will have placed ground

STORAGE MODE

Z — Internal error correction (Offset removal)
1 — Connect first analog value from Analog Storage to A/D Amp
1 — Digitize first digit
1 — Display first digit
1 — Restore first analog value in Analog Storage
1 — Display OUT
1 — Reset Counter
2 — Connect second analog value from Analog Storage to A/D Amp
2 — Digitize second digit
2 — Display second digit
2 — Restore second analog value in Analog Storage
2 — Display OUT
2 — Reset Counter
3 — Connect third analog value from Analog Storage to A/D Amp
3 — Digitize third digit
3 — Display third digit
3 — Restore third analog value in Analog Storage
3 — Display OUT
3 — Reset Counter
4 — Connect fourth analog value from Analog Storage to A/D Amp
4 — Digitize fourth digit
4 — Display fourth digit
4 — Restore fourth analog value in Analog Storage
4 — Display OUT
4 — Reset Counter

NOTE: Depending on the state of the Measure Store Multivibrator the instrument will return to "Z" time and in Measure Mode or recycle in Storage Mode.

Figure 7. 8100 DISPLAY SEQUENCE, STORAGE MODE

potential on the 5 lines to the readout tubes. Q68 and Q72 will be enabled by the 1 pulse and clock pulse during the second half of the time period. This applies the +200 volts to V2 causing it to display the digit 5.

During the 3 time period, Q32 will be enabled placing the .3 volts stored in C32 to be applied to the A-D Amplifier. The output of the amplifier will exceed the 7 volt reference and Q89 will supply current to the VCO which produces a pulse train. The pulses will be counted and translated to BCD output. This BCD output will cause the ladder switches to operate and cause the output of both ladders to increase by .1 volt for every pulse of the VCO. When the output of the Primary Ladder reaches .3 volts the A-D Amplifier will be satisfied and its output will drop below 7 volts causing Q89 to stop conducting, and the VCO will stop pulsing. The output of the Secondary Ladder (.3 volts) will be stored on C32 during the second half of the time period through Q28 which conducts only during the second half of each time period.

The Decoder Driver will have translated the BCD output to decimal and placed ground potential on all of the 3 lines to the readout tubes. Q69 and Q73 will have been enabled, during the second half of the time period, by the 3 time pulse and the clock pulse and the 3 will be displayed by V3.

Time pulse 4 will cause the .2 volts on C33 to be placed on the input to the A-D Amplifier whose output will exceed the 7 volt reference. Q89 will conduct and the VCO will pulse causing the ladder outputs to step .1 volt for every pulse received. When the output of the Primary Ladder, which is fed back to the summing point, reaches .2 volts, the output of the amplifier will no longer be higher than the 7 volt reference and Q89 will stop supplying current to the VCO. The Secondary Ladder will charge C33 to .2 volts and the action of the Decoder Driver will cause ground potential to appear on all of the 2 lines to the readout tubes. Q70 and Q74 will be enabled during the second half of the time period, at which time V4 will display the 2.

SUMMARY:

The capacitors in the Analog Storage Circuit will contain all of the increments of the voltage that were digitized during the previous Measurement Cycle. The Sample and Hold Circuit is disabled during all Storage Cycles. Each digit is displayed only during the last half of each time period. During the Storage Cycle the Polarity Sensing Circuit is not enabled.

This completes the Storage Cycle and as previously explained, the instrument will enter another Storage Cycle unless the charge on capacitor C29 has decreased to a value low enough to cause the Measure Store Multivibrator to pulse. If the Multivibrator does pulse a new Measurement Cycle will start and the input will be sampled again.

TROUBLESHOOTING: (Figure 8)

1. There are several ways of isolating the section of the 8100 that is malfunctioning. Observation of the readout and logical deduction based upon the knowledge of the theory of operation may be adequate to sectionalize the trouble.

2. The Power Supplies are interrelated and to isolate troubles in this area it may be necessary to isolate the −18 volt supply. To do this, disconnect the +15 volt end of R5 and connect it to an external source, or disconnect R35 and place a 1330Ω ±1% resistor from the base of Q3 to ground.

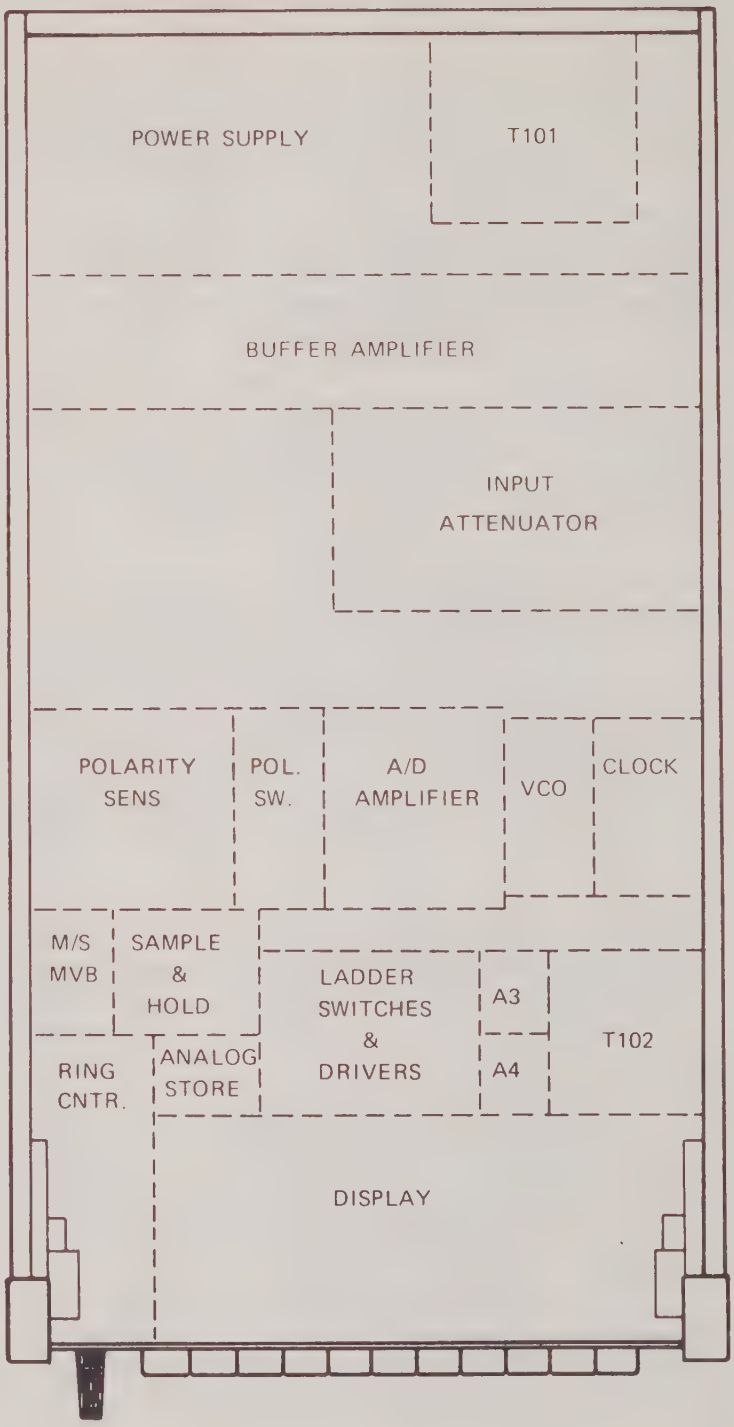


Figure 8. 8100 LAYOUT

3. The Input Buffer can be checked by measuring the voltage between TP9 and TP1 (ground), while measuring a voltage in the 1 Volt DC range. The voltage measured should be the same as the input but in reverse polarity.

4. The Auto Zero circuit will mask many types of trouble, so to disable this circuit it will be necessary to jumper TP6 to TP7 and jumper −18 volts to TP8. The measurement will now have an offset but the Auto Zero will be disabled.

5. Storage Mode can be avoided and the instrument placed in continuous Measurement Mode by placing a jumper between TP4 and TP5.

6. Connect +15 volt supply to the junction of R60 and R61, the Ring Counter will stop and the instrument will no longer display anything in the readout tubes. All of the output lines should measure −18 volts at this time. Remove the jumper and measure the collector voltage with an oscilloscope, each collector should measure about .3 volts when the transistor conducts.

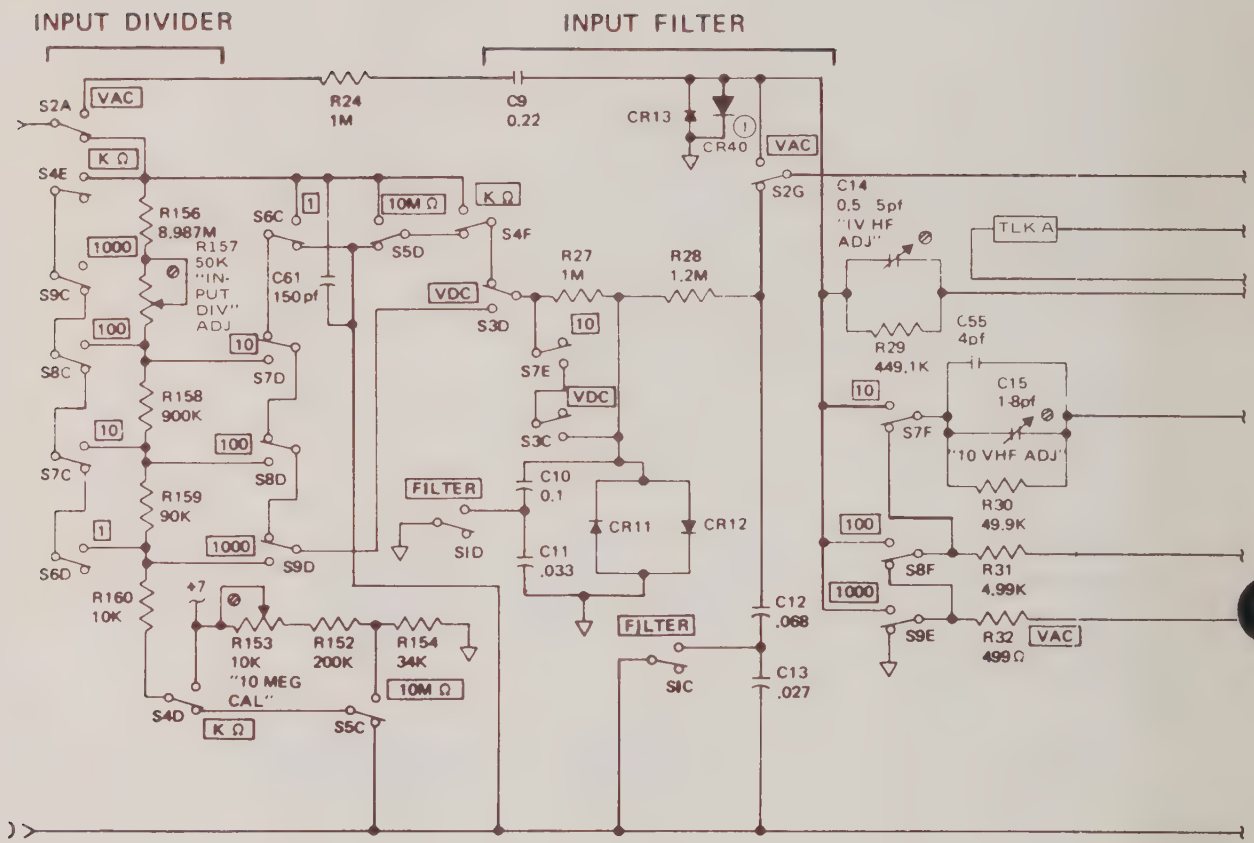
7. An excessive load on any Ring Counter output can cause it to oscillate. Spikes following the time pulse indicate that the Ring Counter is near oscillation.

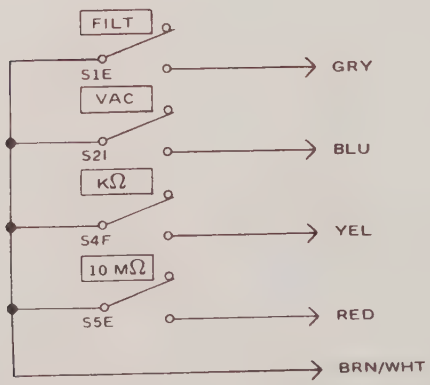
8. Trailing edge droop on the time pulses is caused by low gain transistors Q20 through Q28.

9. The following procedure will check the operation of the A-D Amplifier:

   a. Disable the Ring Counter by placing a jumper from +15 volts to TP11.
   b. Disable the Measure Store Multivibrator by placing a jumper from TP4 to TP5.
   c. Enable the Polarity Sense by placing a jumper from Q13 source to Q13 drain.
   d. Remove Binary Counter A4.
   e. Measure the voltage between TP2 and TP1 (ground).
   f. Apply 100 mv increments of input to the 8100. The measured voltage should increase 350 mv for every 100 mv increment of input and will be of the same polarity.

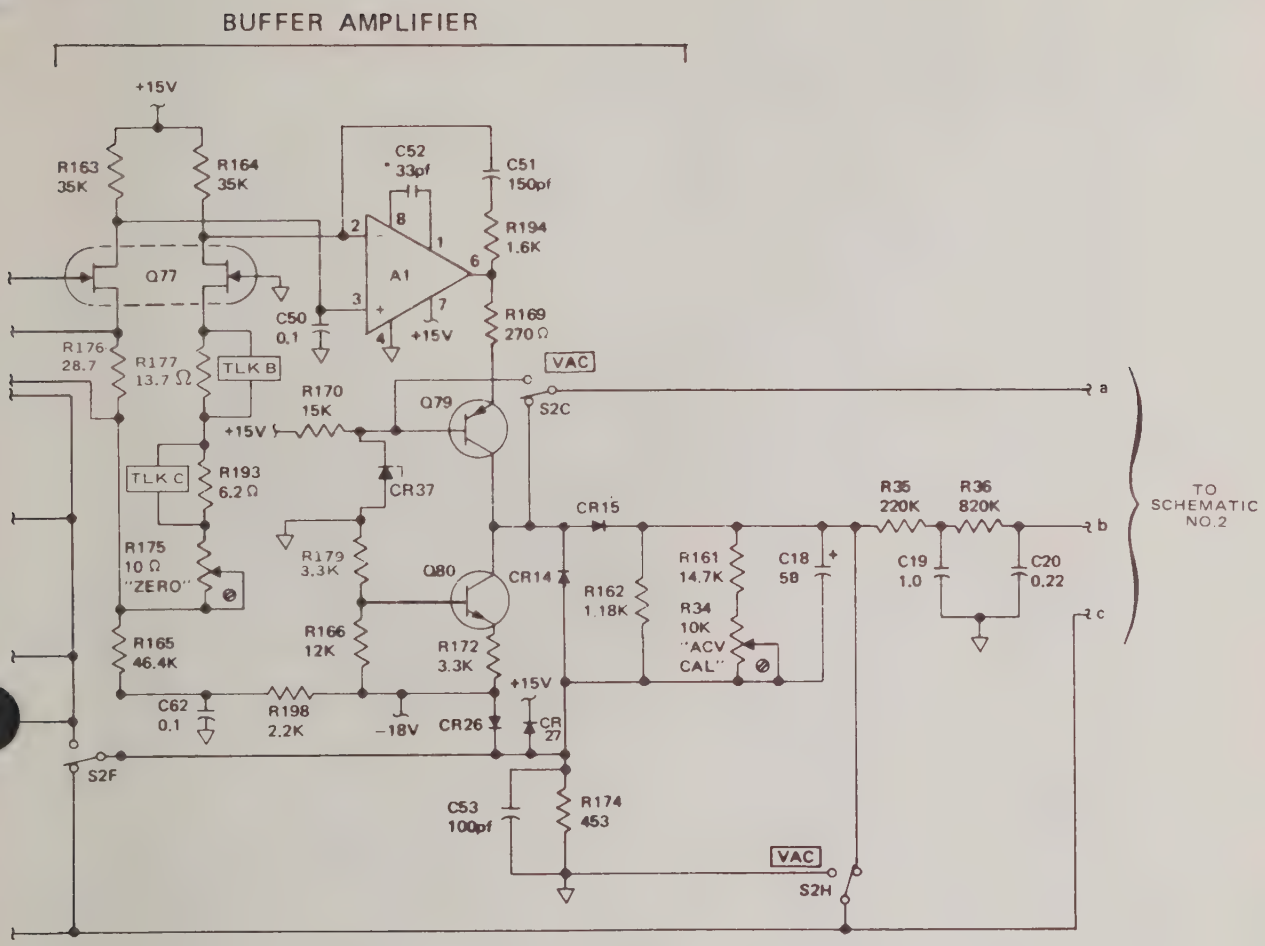
BUFFER AMPLIFIER





CHANGES:

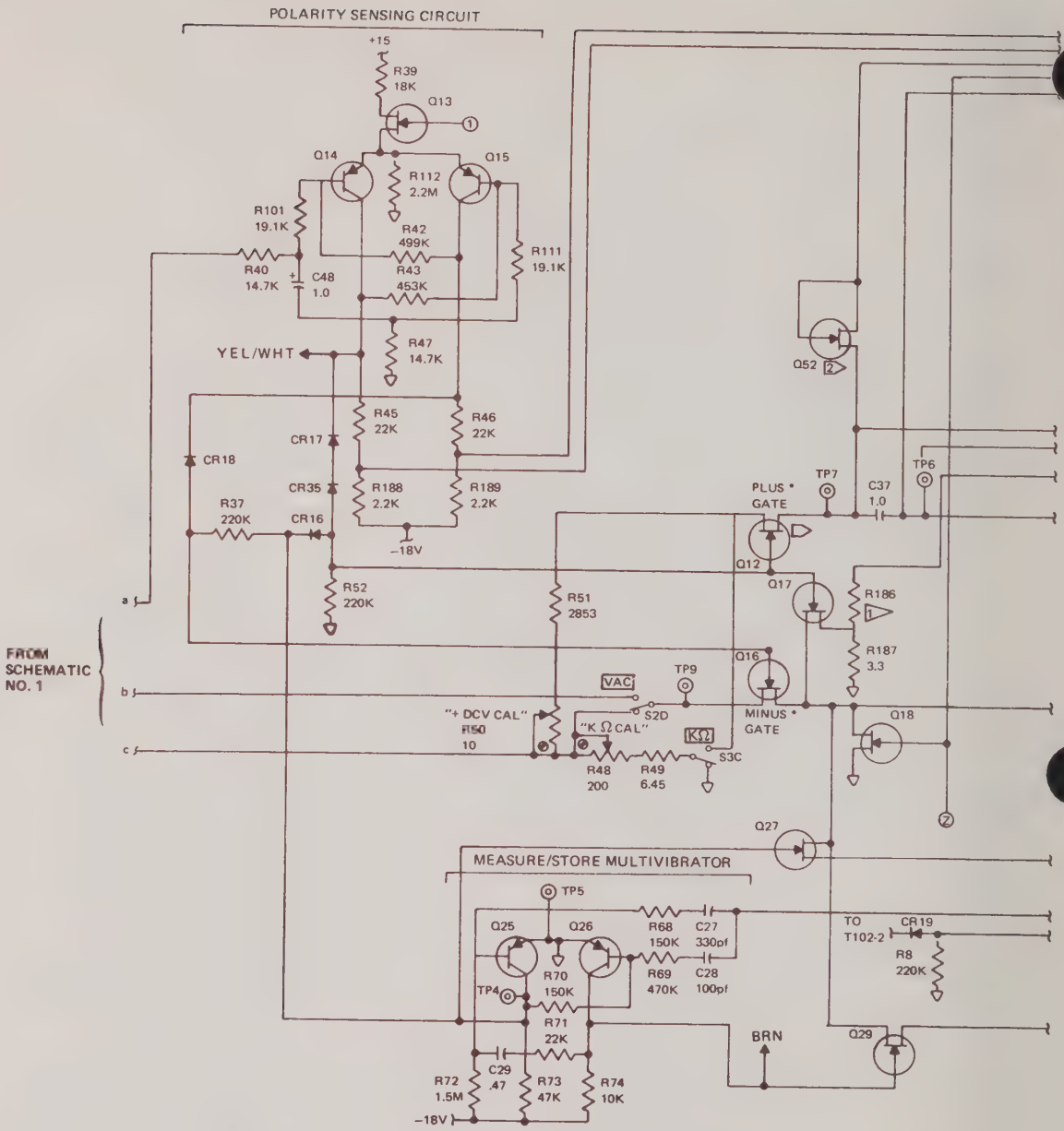
(1) CR40 ADDED AT S/N 2500 AND ON.



NOTES;

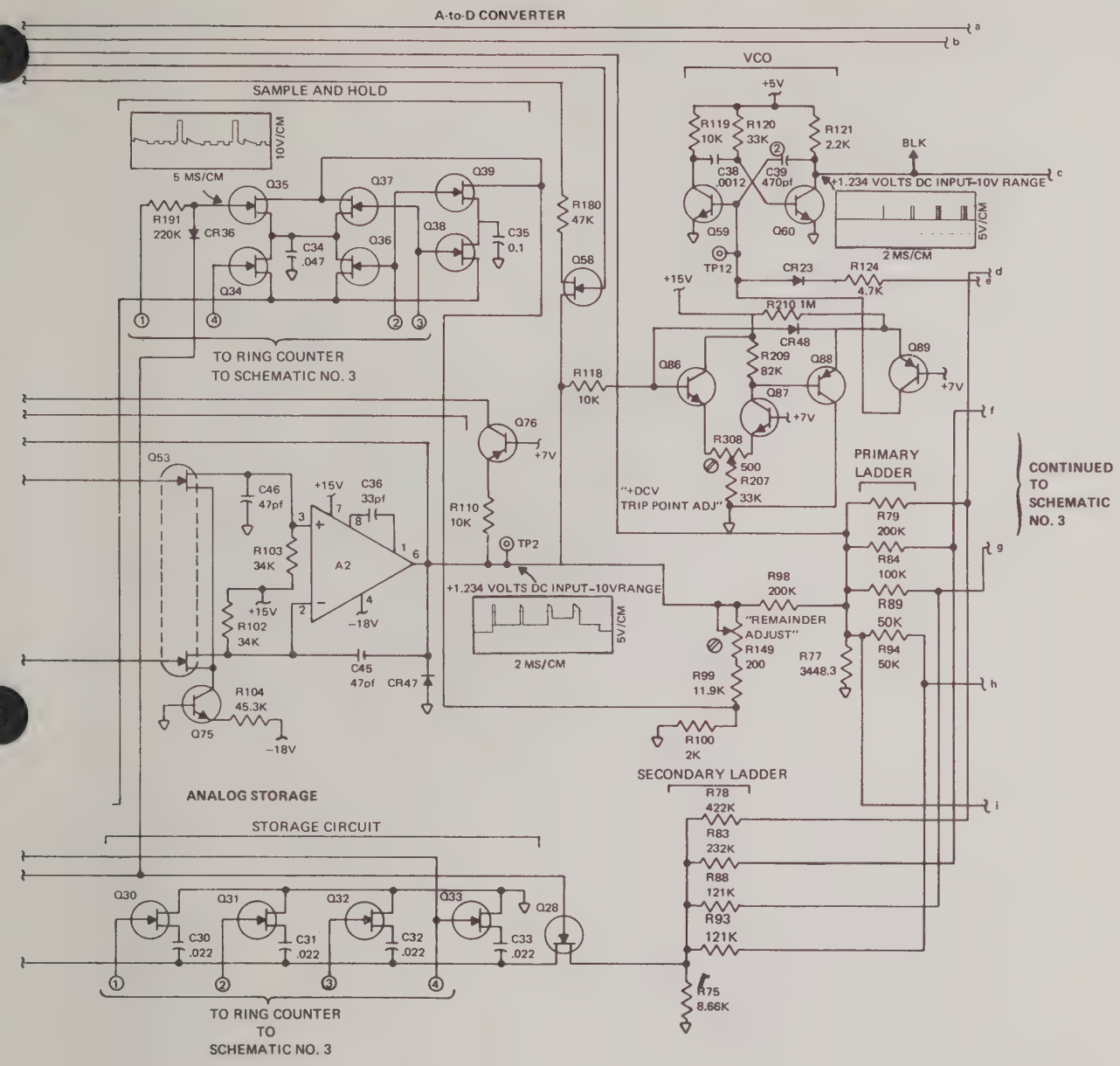
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.
5. TLK TEST LINK.
6. ⟶ (COLOR) CONNECTORS FOR ISOLATED PRINTER OUTPUT OPTION (-02).

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A DIGITAL MULTIMETER SCHEMATIC NO. 1	
SER. NO. 123 THRU 3409 AND 3420 THRU 4097	REV d
FLUKE JOHN FLUKE MFG. CO., INC P.O. Box 7428 Seattle, Washington 98133	



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.
5. TLK TEST LINK.
6. 1 R186 SELECTED IN FINAL CALIBRATION.
7. (COLOR) CONNECTORS FOR ISOLATED PRINTER OUTPUT OPTION (-02).



8. READOUT TUBE IN PIN LAYOUT:

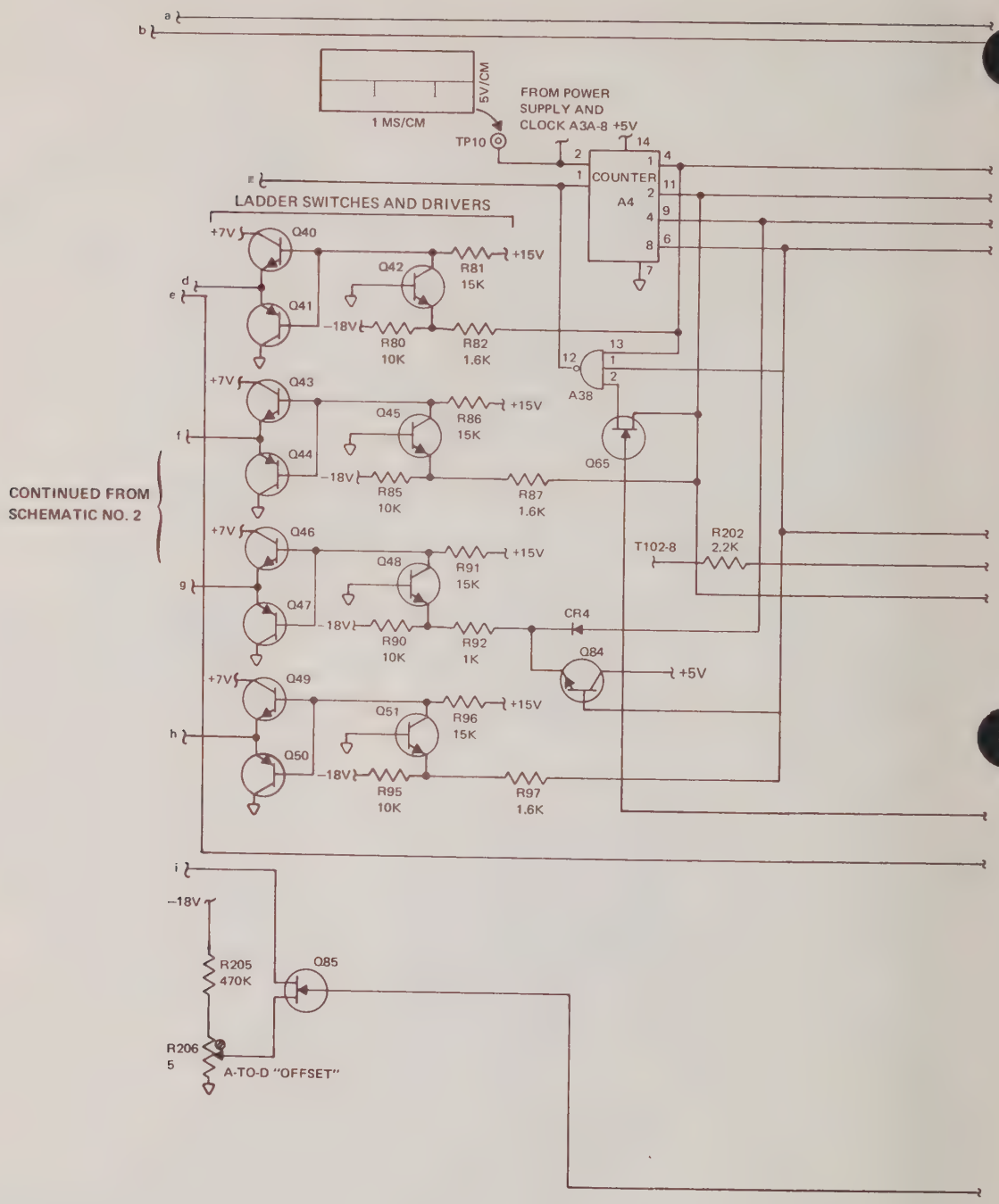
	1° °0	
	2° °9	
	3° °A	
RHD°	4° °8	°LHD
	5° °7	
	6° °A	

BOTTOM VIEW

9. °PLUS GATE ON WITH POSITIVE INPUT; MINUS GATE ON WITH NEGATIVE INPUT.

10. [2] MATCHED FET PAIR.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A DIGITAL MULTIMETER SCHEMATIC NO. 2	
SER. NO. 3410 THRU 3419 AND 4098 AND ON	REV. —
JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

2. ALL SWITCHES SHOWN IN OFF POSITION.

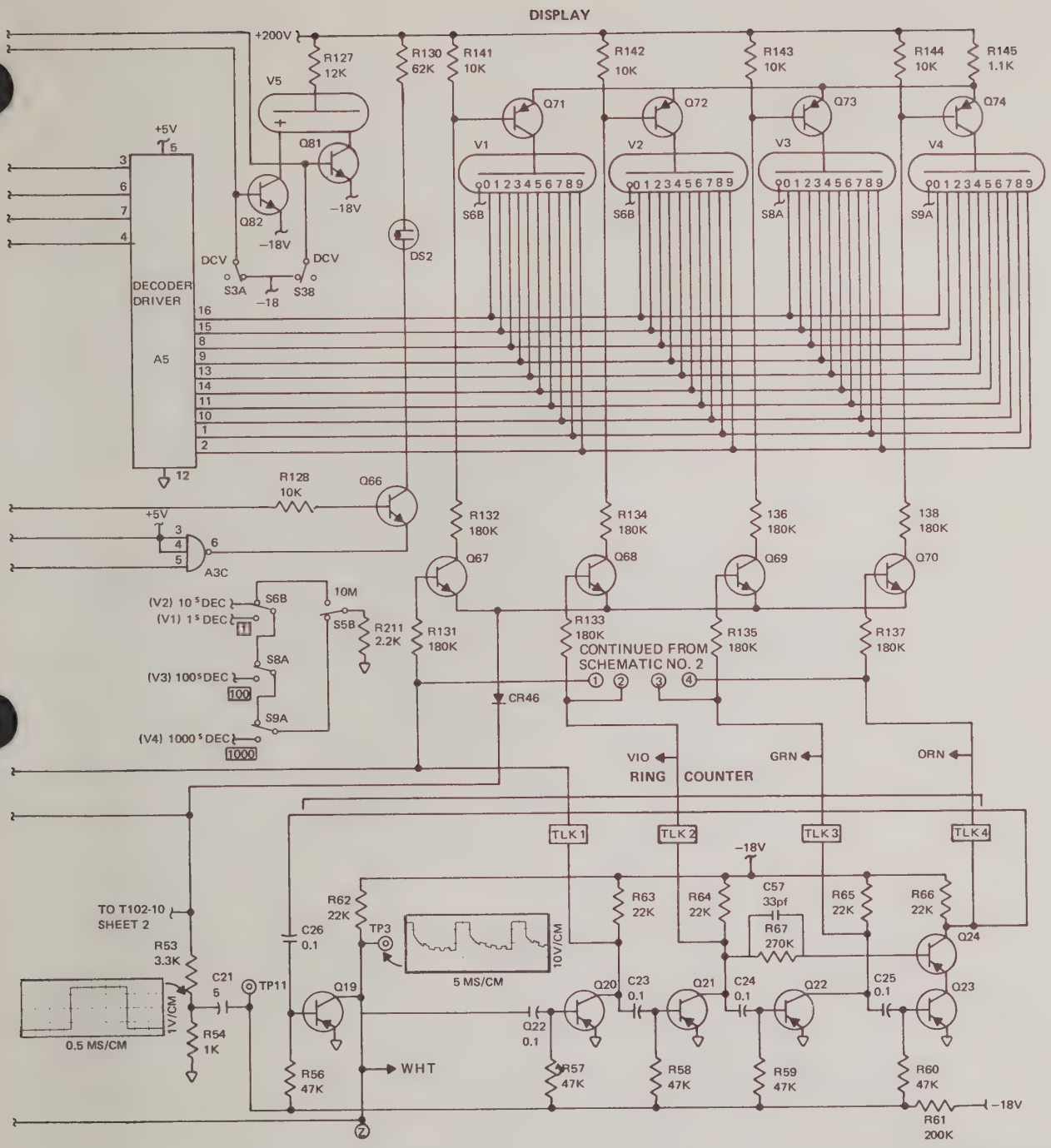
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.

4. ▭ DENOTES FRONT PANEL LOCATION.

5. [TLK] TEST LINK

6. [1] R186 SELECTED IN FINAL CALIBRATION.

7. ⟶ (COLOR) CONNECTORS FOR ISOLATED PRINTER OUTPUT OPTION (–02).



8. READOUT TUBE IN PIN LAYOUT:

	1°	°0
	2°	°9
	3°	°A
RHD°	4°	°8 °LHD
	5°	°7
	6°	°A

BOTTOM VIEW

9. *PLUS GATE ON WITH POSITIVE INPUT; MINUS GATE ON WITH NEGATIVE INPUT.

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8100A

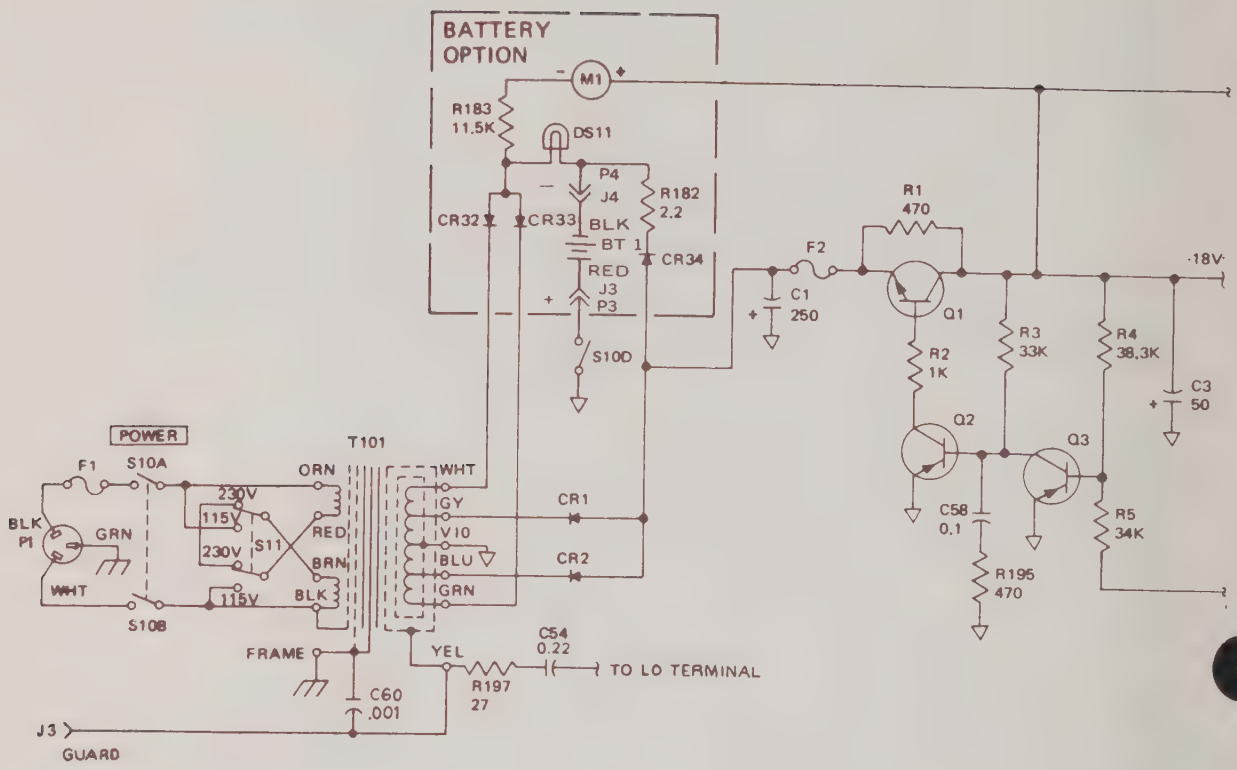
DIGITAL MULTIMETER

SCHEMATIC NO. 3

SER. NO. 3410 THRU 3419 AND 4098 AND ON

REV —

FLUKE JOHN FLUKE MFG. CO., INC.
P.O Box 7428 Seattle, Washington 98133



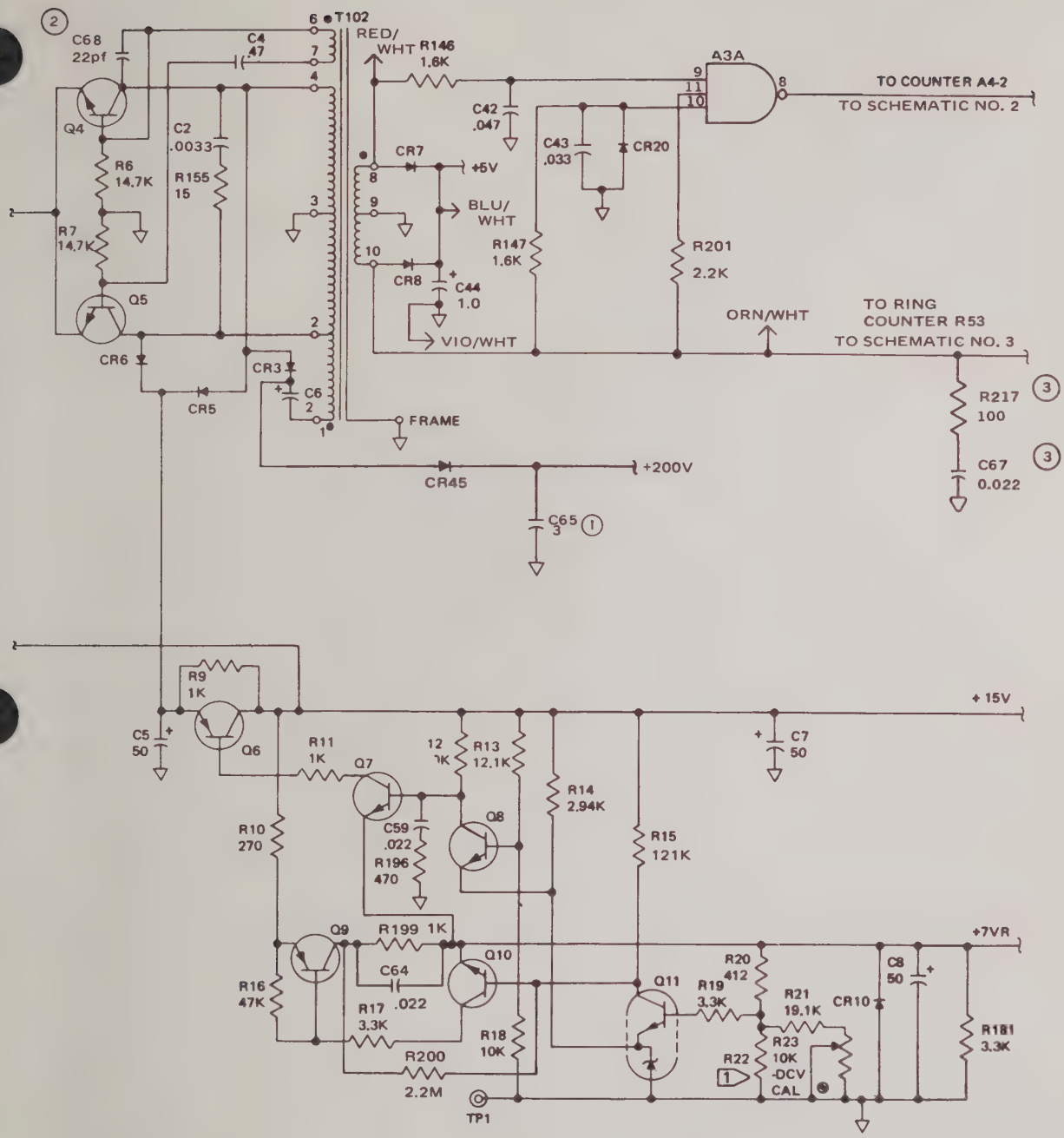
NOTES :

1. [1] VALUE SELECTED AT TEST OF Q11

CHANGES:

(1) FOR S/N 3410 THRU 3419, 4098 THRU 4365, & 4429 THRU 4477: C65 WAS 4uf.

(2) C68 ADDED S/N 5050 AND ON.



FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A DIGITAL MULTIMETER SCHEMATIC NO. 4	
SER. NO. 3410 THRU 3419 AND 4098 AND ON	REV. -
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	

(3) R217 AND C67 ADDED S/N 5018 AND ON.

(4) →(COLOR) CONNECTORS FOR ISOLATED PRINTER OUTPUT OPTION (–02).